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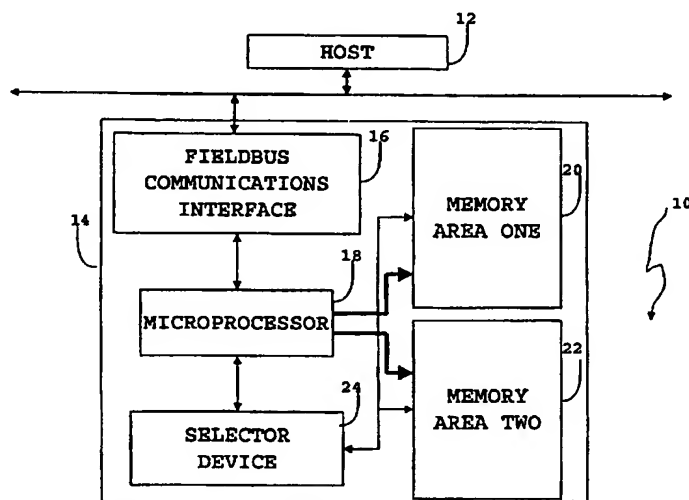
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(54) Title: FIELDBUS UPGRADABLE APPARATUS AND METHOD



(57) Abstract: A method to modify control devices residing on a Fieldbus communications network, without interrupting the operation of the control devices. The control device updating may further be controlled and monitored by a remotely located host. The control device comprises at least two distinct memory areas wherein at least one memory area must be active, and at least one memory area must be inactive. Active memory areas provide the control device microprocessor operating system with executable instructions or data. The host downloads new executable instructions or data to inactivate memory areas, with associated data entry points, during unscheduled communications periods. Upon a full data transfer and proper verification of the new data, the host causes a selector device to activate the previously inactive memory area by directing the microprocessor to the entry points of the newly downloaded executable instructions or data. The memory activation must occur while the microprocessor is idle.

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3                   FIELDBUS UPGRADABLE APPARATUS AND METHOD  
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5                   CLAIM OF PRIORITY

6           This application claims priority to provisional application  
7   U.S.S.N. 60/136,253, entitled FIELDBUS UPGRADABLE DEVICE, and  
8   filed on May 27, 1999, naming VLADIMIR KOSTADINOV as inventor,  
9   the contents of which are herein incorporated by reference.  
10

11                   BACKGROUND OF THE INVENTION

12       (1) Field of the Invention

13           The present invention relates generally to communications  
14   systems, and more particularly to utilizing communications  
15   systems for uninterrupted software upgrading.

16       (2) Description of the Prior Art

17           In the manufacturing and process control industries, there  
18   is a continuing effort to eliminate older, centralized plant  
19   control strategies, in favor of standard protocols. This type of  
20   control provides true device interoperability, enhanced field-  
21   level control, and reduced installation costs.

22           The inherent modularity and intrinsic software reliance of  
23   modern manufacturing and process control systems allows a  
24   platform wherein distributed control may be best utilized.  
25   Communications protocols such as the commonly known Fieldbus

1 technology allow for the interconnecting of measurement and  
2 control equipment such as sensors, actuators, and controllers.  
3 Examples of some Fieldbus technologies include Profibus™ and  
4 Foundation™. Fieldbus is an all-digital, serial, two-way  
5 communications system that serves as a Local Area Network (LAN)  
6 for instruments in process control and manufacturing automation  
7 applications. Fieldbus facilitates the distribution of the  
8 control application across the network. Control through the  
9 network is particularly advantageous when the devices or  
10 processes to be controlled are physically remote from a central  
11 control station.

12 Although the systems, sensors, and devices of such  
13 manufacturing and process systems are modular, and there are  
14 communications standards for interconnecting components of such  
15 systems, there is currently no method or apparatus for allowing  
16 device, system, or sensor software upgrades from remote locations  
17 without interrupting the control system.

18 What is needed is a method and apparatus that facilitates  
19 uninterrupted and remote upgrade of specified control system  
20 components.

#### 21 SUMMARY OF THE INVENTION

22 It is one aspect of the present invention to provide a  
23 method and system for utilization with the well-known Fieldbus  
24 communication protocol, that allows uninterrupted software  
25

1 upgrading of remote, microprocessor controlled devices that exist  
2 on the Fieldbus network.

3 In a preferred embodiment, the Fieldbus network comprises a  
4 plurality of control devices, wherein control devices may be  
5 input devices, output devices, or input/output devices. Each  
6 control device may be configured for Fieldbus communications.  
7 Each control device also comprises at least two memory areas  
8 within which executable software and data may reside, wherein at  
9 least one memory area may be active and at least one memory area  
10 may be inactive. Memory areas may further comprise multiple  
11 memory segments. Each control device additionally comprises a  
12 selector device that specifies to the microprocessor those memory  
13 areas that are active. In a preferred embodiment, the selector  
14 device directs the control device microprocessor to the active  
15 memory areas during the microprocessor operating system cycle.

16 It is another aspect of the present invention to allow a  
17 Fieldbus communications system wherein a host computer configured  
18 within the Fieldbus network may provide software upgrades and  
19 other control to remote control devices through the network. In  
20 an embodiment, software upgrades are performed without  
21 interrupting the control device processor, by issuing a Fieldbus  
22 compatible command that indicates to the control device  
23 microprocessor that a new software version is available for the  
24 designated control device. The respective microprocessor routes  
25 the software upgrade to a presently inactive memory area within

1 the designated control device that shall be designated the new  
2 memory area. Such transfer occurs during otherwise unscheduled  
3 communications periods to avoid interruption to the network or  
4 the control device. Similarly, the remotely located control  
5 device microprocessor performs the transfer without interrupting  
6 the presently executing application or data functions in the  
7 control device. The microprocessor also verifies the new  
8 software. The new memory area may be activated during a  
9 microprocessor idle period by directing the microprocessor to the  
10 new software, thereby providing a seamless transition to the new  
11 memory area and hence the new software.

12 It is another aspect of the invention to provide a mechanism  
13 whereby the host may return the microprocessor to a previously  
14 active memory area within a designated control device.

15 It is yet another aspect of the invention to utilize new  
16 memory areas for increasing the control device functionality.  
17 The number of active memory areas may increase as functionality  
18 is increased.

19 Other objects and advantages of the present invention will  
20 become more obvious hereinafter in the specification and  
21 drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the invention and many of the attendant advantages thereto will be readily appreciated as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings, wherein like reference numerals refer to like parts and wherein:

FIG. 1 is a representative block diagram of a Fieldbus communications network segment displaying a host and a single control device;

FIG. 2 presents a control device initialization methodology;

FIG. 3 diagrammatically represents the logic for altering control device memory; and,

FIG. 4 presents the microprocessor operating system and unscheduled communications timelines.

DESCRIPTION OF THE PREFERRED EMBODIMENT

To provide an overall understanding of the invention, certain illustrative embodiments will now be described; however, it will be understood by one of ordinary skill in the art that the systems described herein can be adapted and modified to provide systems for other suitable applications and that other additions and modifications can be made to the invention without departing from the scope hereof.

1 Referring now to FIG. 1, there is shown a block diagram of a  
2 system 10 that incorporates an embodiment of the invention. The  
3 FIG. 1 system 10 comprises a host 12 that is configured for  
4 communications using the well-known Fieldbus communications  
5 protocol. The host 12 can be implemented using a digital  
6 computer system that may be any microprocessor-based system  
7 including a computer workstation, such as a PC workstation, SUN  
8 workstation, handheld or laptop computer, that comprises a  
9 program for organizing and controlling the digital computer  
10 system to operate according to the invention. Additionally and  
11 optionally, the microprocessor-based system can be equipped for  
12 processing multimedia data, and can be, for example, a  
13 conventional PC computer system with a sound and video card. The  
14 computer system can operate as a stand-alone system when not  
15 operating as part of a networked computer system. The host may  
16 therefore be any microprocessor-based device that is designated  
17 to perform the functionality herein to uninterruptively upgrade  
18 software on a specified control device, such specified control  
19 device including, for example, a field device such as a  
20 controller, transmitter, or actuator.

21 The host 12 may provide and receive remote command and  
22 control information to and from a plurality of control devices  
23 residing on the network. FIG. 1 displays a representative  
24 control device 14. The host 12 and control device 14 may not be  
25 co-located on the same Fieldbus segment, and communications

1 between the host 12 and control device 14 may be coupled through  
2 various Fieldbus and other network segments, that shall be  
3 referred to herein collectively as the Fieldbus communications  
4 network.

5 Control devices may be input devices, output devices, or  
6 input/output devices as commonly known in the art. As indicated  
7 by FIG. 1, the control device comprises a Fieldbus communications  
8 interface 16 to receive and transmit commands and data across the  
9 Fieldbus network, at least one microprocessor 18 to execute  
10 control device resident applications and communicate with the  
11 host and other control devices, at least two memory areas 20, 22  
12 for storing executable programs and/or data that may be accessed  
13 by the microprocessor 18, and a selector device 24 interfaces the  
14 microprocessor 18 to executable instructions or data in the  
15 memory areas 20, 22.

16 In a preferred embodiment, the memory areas 20, 22 may be  
17 flash memory, although other memory devices may be utilized  
18 without departing from the invention. Each memory area 20, 22  
19 may additionally be continuous, partitioned, or segmented. The  
20 FIG. 1 memory areas 20, 22 therefore merely represent logically  
21 separate memory areas, and each memory area 20, 22 may be  
22 comprised of memory across multiple segments, etc.

23 For the purposes of this invention, all references to the  
24 microprocessor 18 shall be understood to refer to the embedded  
25 software or operating system that forms a microprocessor



1 operating system, wherein such an operating system is commonly  
2 known for scheduling and executing applications, allocating  
3 resources, etc. In a preferred embodiment, the microprocessor 18  
4 repeatedly performs a scheduled series of tasks during a fixed  
5 time period. The tasks are identified to the microprocessor 18  
6 through entry points that specify a memory area, wherein the  
7 memory area comprises executable instructions or data to perform  
8 and/or complete the task. In an embodiment, the memory area may  
9 comprise executable instructions or data relating to a control  
10 device application.

11 For purposes of this invention, each such repetitive fixed  
12 time period wherein the microprocessor performs the scheduled  
13 tasks shall be defined as a macrocycle. Additionally, any time  
14 within the macrocycle during which the microprocessor is not  
15 executing an application, performing application-dependent  
16 input/output, or performing application related communications,  
17 shall be defined as an idle period.

18 As FIG. 1 indicates, the microprocessor 18 may access the  
19 memory areas 20, 22 in two manners for two distinct purposes.  
20 The microprocessor connection to the memory areas 20, 22 through  
21 the selector device 24 represents the selector device  
22 functionality to supply the microprocessor 18 with entry points  
23 for application executable instructions or data, wherein such  
24 application instructions or data resides in the memory areas 20,  
25 22. For the purpose of this invention, such activity shall be

1 defined as "executable" activity, wherein the microprocessor 18  
2 executes the instructions or data residing in the memory areas  
3 20, 22.

4 Alternately, the microprocessor 18 may directly access the  
5 memory areas 20, 22 (i.e., without selector device 24  
6 intervention) to perform functions unrelated to application or  
7 data execution. Examples of such functions include data  
8 integrity checks, data loading or unloading, etc. For purposes  
9 of this invention, such activity shall be defined as "processing"  
10 activity, wherein the microprocessor 18 processes the memory area  
11 contents without executing the instructions or data therein.

12 The selector device 24 may designate an active memory  
13 area(s) from an inactive memory area(s) for the microprocessor  
14 18. For the purposes of this invention, active memory areas  
15 shall be defined as the memory areas that the microprocessor 18  
16 is directed to, by the selector device 24, to obtain executable  
17 instructions or data. In a preferred embodiment, the selector  
18 device 24 activates a memory area merely by providing the  
19 microprocessor 18 with the entry points to the memory area.

20 For purposes of this invention, all memory areas other than  
21 the active memory areas shall be known as inactive memory areas.

22 The microprocessor 18 does not execute instructions or data from  
23 any inactive memory area, however the microprocessor may process  
24 the inactive memory area contents for data integrity, perform  
25 data downloading, etc.

1           For purposes of this invention, a new memory area shall be  
2 defined as an inactive memory area to which upgradeable  
3 executable instructions (e.g., an application) or data shall be  
4 directed, wherein such upgradeable instructions or data shall  
5 also be referred to collectively as new data. New data may work  
6 independently, to the exclusion of, or together with, existing  
7 data in active memory areas.

8           In a preferred embodiment, the selector device 24 is  
9 incorporated as a software module that interacts with the  
10 microprocessor 18 and may be implemented through software using  
11 higher-level languages such as C++ or Java, or optionally  
12 microcode or machine level instructions; however, those with  
13 ordinary skill in the art shall recognize that the selector  
14 device 24 may be implemented in hardware without departing from  
15 the scope of the invention herein.

16           Referring now to FIG. 2, there is shown a representative  
17 process 40 by which a control device may be initialized. In an  
18 embodiment presented in FIG. 2, upon initialization, the control  
19 device cycles through all control device memory areas and sets to  
20 active all memory areas that are verified through the  
21 verification process. In such an embodiment, the control device  
22 microprocessor selects, in a logical order, a memory area 42.  
23 The microprocessor may then verify 44 the memory area contents  
24 using such well-known techniques as CRC computations, although  
25 the invention is not limited by such verification technique. If

1 the verification fails, the memory area may be marked as inactive  
2 46, and another memory area is selected 42. In a preferred  
3 embodiment, such inactive designation 46 may be a passive  
4 activity since all memory areas other than the active memory area  
5 may be by default, inactive; however, alternate embodiments may  
6 otherwise designate inactive memory areas using alternate  
7 techniques without departing from the invention herein.

8 Alternately, when a memory area is properly verified, a data  
9 area may be assigned 48 within the memory area, and the memory  
10 area may be designated active 50. The next memory area in the  
11 logical order may then be selected 42, until all such memory  
12 areas are designated active or inactive.

13 Although FIG. 2 presents an initialization process for one  
14 embodiment wherein multiple memory areas may be active, alternate  
15 embodiments may utilize different initialization processes. In  
16 applications wherein only one memory area may be allowed to be  
17 active, such memory area may be "selected" 42 by the respective  
18 selector device or microprocessor that may retain or preserve the  
19 active and inactive memory area status data from a previous  
20 session. In yet another embodiment, the host may store the  
21 location of the active memory areas for each control device, and  
22 transmit, using the Fieldbus protocol, the active memory  
23 address(es) to the respective control device upon initialization.

24 Referring now to FIG. 3, there is shown a process 60 wherein  
25 new executable instructions or data may be provided to a

1 designated control device. In the FIG. 3 embodiment, updating  
2 the control device comprises downloading new data. The host may  
3 request an upgrade to the control device, and the request may be  
4 communicated between the host and control device using Fieldbus  
5 protocols. As FIG. 1 indicates, communications between the host  
6 and the control device require communication through the Fieldbus  
7 interface, that thereafter interacts with the microprocessor that  
8 processes the commands. Such communications may occur during  
9 otherwise unscheduled communications periods between the host and  
10 control device, wherein unscheduled communications periods may be  
11 defined as those time periods during which the control device  
12 microprocessor may not be previously scheduled to exchange  
13 input/output data relating to applications executing on the  
14 control device. Such previously scheduled input/output periods  
15 may comprise communications between the control device and the  
16 host, or between the control device and another control device.

17 The host may identify the control device through a user-  
18 interface or other interactive mechanism that allows a host  
19 operator to designate a specific control device. In a preferred  
20 embodiment, the host comprises a user interface that similarly  
21 indicates respective active and inactive memory areas for  
22 specified control devices. The host may store information  
23 regarding the present active memory areas for a specified control  
24 device and display such information to the host user, or  
25 alternately, the host may poll the selector device of the

1 specified control device, using the Fieldbus protocol, to  
2 ascertain the present active memory areas. In yet another  
3 embodiment, the selector device may provide the host with the  
4 active memory area designation upon completion of the control  
5 device initialization processing as indicated by FIG. 2.

6 In a preferred embodiment, the host user interface may allow  
7 a host operator to specify an inactive memory area as a target  
8 for the new data. Such user interface may also allow the host  
9 operator to specify the new data. Referring back to FIG. 3, the  
10 host may then issue, using Fieldbus communications protocols, a  
11 data download request 62 that may be received by the specified  
12 control device microprocessor to cause the new memory area  
13 identifier and new data to be transmitted to the control device.

14 In a preferred embodiment, the host also transfers the new  
15 memory area entry points, wherein the entry points shall direct  
16 the microprocessor to the executable instructions or data in the  
17 new memory area. Such host requests and transfers are also  
18 performed during previously defined unscheduled communications  
19 intervals.

20 Upon receipt 64 of the download request and new memory area  
21 designation, new data, and new memory area entry points, the  
22 microprocessor may direct the new data to the new memory for  
23 storage. The microprocessor may also direct the new memory entry  
24 points to the selector device for storage. The host may then  
25 issue a verification command that may cause the control device

1 microprocessor to verify 66 the new data in the new memory area,  
2 wherein such verification may be, for example, a CRC computation,  
3 but the invention herein is not limited to such verification  
4 method. In an embodiment, the microprocessor stores the result  
5 of such memory verification in the selector device. In a  
6 preferred embodiment, the microprocessor functions of receiving  
7 64, redirecting 64, and verifying 66 the new data, may be  
8 performed in parallel processes with the presently executing  
9 applications in the active memory areas. Such functions may  
10 therefore be performed at any time in the microprocessor  
11 timeline, other than the during scheduled input/output network  
12 communications intervals.

13 If a proper verification of the new memory area is not  
14 achieved 68, the host may issue another download request, again  
15 designating a new memory area and the new data. The same  
16 inactive memory area may be utilized, or the host may request a  
17 different memory area if more than one inactive memory areas  
18 exist.

19 Alternately, upon proper verification of a memory area, the  
20 control device microprocessor may inform the host of the proper  
21 verification, wherein the host may request that the new memory be  
22 designated an active memory 70.

23 The control device microprocessor, upon receiving a request  
24 from the host to change the status of an inactive (i.e., new)  
25 memory area to active, may interrogate the verification status of

1 the new memory 72. Alternately, the microprocessor may  
2 interrogate whether entry points are received for the new memory  
3 area. If the new memory area is not verified, or entry points do  
4 not exist, the microprocessor may reject 74 the host request to  
5 change the active memory designation. Alternately, if the new  
6 memory is verified and entry points are stored, the host's  
7 request may be granted, and the microprocessor may inform the  
8 selector device that the new memory area may be activated 76.

9 Depending upon, for example, whether the new data comprises  
10 cooperative as compared to replacement data, the host may issue a  
11 request to inactivate a presently active memory area 78. In some  
12 embodiments, activating and inactivating memory areas may require  
13 proper coordination and timing to achieve the desired  
14 microprocessor direction via the selector device-provided entry  
15 points.

16 In one embodiment wherein the system is initialized through  
17 the cyclic process depicted in FIG. 2, memory inactivation may  
18 cause the memory area to purposefully fail subsequent  
19 verification checks. In such a system, re-activating the content  
20 of that memory segment may require a new download of the older  
21 executable instructions or data. Alternately, the inactivation  
22 process may be reversible with another command from the host,  
23 thereby preventing the necessity for another data download.

24 In embodiments wherein only one memory area can be active,  
25 the inactivation process may be simplified and may be implemented



1 using default logic embedded in software or hardware. All such  
2 activation and inactivation methods and processes may be  
3 implemented in various manners without departing from the scope  
4 of the present invention.

5 The method of indicating active or inactive memory areas  
6 relates also to the ability to return to previous versions of  
7 executable instructions or data. For example, if a system  
8 comprises N memory areas, wherein only one memory area may be  
9 active, the system may be implemented such that as many as (N-1)  
10 versions of executable instructions or data may be stored in  
11 inactive memory areas. Such configuration may also allow rapid  
12 transition between these versions of executable instructions or  
13 data by issuing a host request with the new memory area  
14 designation.

15 Alternately, when multiple memory areas are allowed to be  
16 active, the present invention provides a structure wherein  
17 functionality may be easily added or eliminated. Modular  
18 upgrades may also be readily achieved in such an embodiment,  
19 wherein one memory area with a specific functionality may be  
20 upgraded to the exclusion of other active memory areas.

21 Referring now to FIG. 4, there is shown two timelines 80  
22 indicating a representative microprocessor operating system  
23 timeline, previously defined as a macrocycle, and a corresponding  
24 unscheduled communications timeline. As mentioned previously,  
25 the macrocycle 82 may be viewed as a repeatable interval, the

1 duration of which may be designed to allow execution of all  
2 control device applications and input/output functions, with  
3 consideration for the overall communications bandwidth during the  
4 input/output functions. For example, during each representative  
5 macrocycle of FIG. 4, the microprocessor operating system  
6 executes a first application 84, wherein such first application  
7 is followed immediately by a first input/output interval 86.  
8 During the first input/output interval 86, the control device may  
9 transfer data relating to the first application, using the  
10 Fieldbus protocol. Such communications intervals 86 are  
11 therefore known as scheduled communications intervals, and may be  
12 between the control device and the host, or between the control  
13 device and another control device. Upon completion of the first  
14 input/output interval 86, the microprocessor executes a second  
15 application 88, wherein such second application 88 is followed in  
16 time by a second input/output interval 90, such second  
17 input/output interval 90 also being a scheduled communications  
18 interval. Although the representative embodiment of FIG. 4  
19 indicates only two applications, the invention herein is not  
20 limited by the number of applications executed on a control  
21 device during a given macrocycle.

22 Referring again to FIG. 4, the selector device may activate  
23 or inactivate memory areas, or change the entry points, at any  
24 time during the macrocycle that the microprocessor operating  
25 system is not executing applications or utilizing application

1 dependent data. Such periods in the macrocycle are indicative of  
2 the previously defined idle periods 92. During these idle  
3 periods 92, the selector device may incorporate the entry points  
4 to the new memory area such that during the microprocessor's next  
5 scheduled application execution, the new entry points may direct  
6 the microprocessor to the new data. By altering the  
7 microprocessor entry points during intervals wherein the  
8 microprocessor is not performing application or application-  
9 dependent processing, the transition to the new data may occur  
10 without interrupting the microprocessor functionality or  
11 processing timeline.

12 As mentioned previously, activating a memory area may  
13 require inactivating another memory area, and such  
14 activation/inactivation may require coordination. Inactivation,  
15 just as activation, must be performed during the idle periods 92,  
16 when the microprocessor is neither scheduled for application  
17 execution or application input/output. Such  
18 activation/inactivation may require several idle periods to  
19 achieve complete conformance. In an embodiment, the host may  
20 extend an idle period (i.e., prevent the next macrocycle from  
21 commencing) to effectuate a memory area activation or  
22 inactivation.

23 Alternately, data transfers from the host computer to the  
24 new memory area, or any commands or requests from the host, may  
25 be scheduled during the unscheduled communications periods 94.

1 As defined previously, unscheduled communications periods 94  
2 comprise any macrocycle time interval during which the  
3 microprocessor is not performing input/output with the host or  
4 another control device. Unscheduled communications therefore  
5 comprise all time within the processing interval that is not a  
6 scheduled communications interval.

7 As with any communications system, data rates must be  
8 considered when scheduling events. Depending upon the data rates  
9 and the data amount transferred to a new memory area, more than  
10 one macrocycle may be required to download the data; therefore,  
11 the download of executable instructions or data to a new memory  
12 area may occur during one macrocycle, while the verification of  
13 such new memory may not occur until several macrocycles after  
14 such download begins. Further, altering the microprocessor  
15 operating system entry points may require a period greater than a  
16 single idle period 92, thereby delaying the activation of a new  
17 memory area for several macrocycles.

18 In one embodiment where several control devices may be  
19 upgraded, the upgrades may be coordinated to occur at the same  
20 time. In such an embodiment, new data may be downloaded to all  
21 control devices, and respective microprocessors may be redirected  
22 to respective new data memory areas to achieve a synchronized or  
23 otherwise controlled upgrade.

24 In one embodiment, the microprocessor redirection for one or  
25 more control devices may be scheduled to a certain time or event,

1 without departing from the invention. In such an embodiment, one  
2 or more control devices may comprise new data in an inactive  
3 memory area. The host may then monitor at least one parameter,  
4 wherein the parameter(s) may relate to control devices, and upon  
5 the particular parameter(s) attaining a predetermined value, the  
6 host may issue a request to redirect the microprocessor on one or  
7 more control devices.

8 The advantage of the present invention over the prior art is  
9 that control devices within a Fieldbus network may be remotely  
10 updated with new executable instructions or data without  
11 disturbing the operation of the control device.

12 What has thus been described is a method and apparatus to  
13 modify control devices residing on a Fieldbus communications  
14 network, without interrupting the operation of the control  
15 devices. The control device updating may further be controlled  
16 and monitored by a remotely located host that also communicates  
17 on the Fieldbus network. The control device may comprise at  
18 least two distinct memory areas, wherein at least one memory area  
19 must be active, and at least one memory area must be inactive.  
20 Active memory areas provide the control device microprocessor  
21 operating system with executable instructions or data. The host  
22 downloads new executable instructions or data to inactive memory  
23 areas, with associated data entry points, during unscheduled  
24 communications periods wherein data input/output is not being  
25 performed between the control device and the host or another

1 control device. Upon a full data transfer and proper  
2 verification of the new data, the host may issue an activation  
3 command that causes a selector device to activate the previously  
4 inactive memory area by directing the microprocessor to the entry  
5 points of the newly downloaded executable instructions or data.  
6 The memory activation must occur while the microprocessor is not  
7 performing application execution, application input/output, or  
8 application communications. By timing the memory activation in  
9 this manner, the microprocessor may be redirected to the newly  
10 downloaded executable instructions or data without microprocessor  
11 interruption.

12 Although the present invention has been described relative  
13 to a specific embodiment thereof, it is not so limited.  
14 Obviously many modifications and variations of the present  
15 invention may become apparent in light of the above teachings.  
16 For example, the selector device functionality may be performed  
17 in hardware or software. The selector device may be incorporated  
18 within the microprocessor or independent of the microprocessor  
19 operating system. The Fieldbus network may contain any number of  
20 control devices. Each control device may have a different  
21 macrocycle length during which a varying number of applications  
22 may be executed. Depending on the network size, there may be  
23 more than one host. The host and the control devices may reside  
24 on different Fieldbus segments, wherein such segments may be  
25 connected through otherwise compatible network software or

1 hardware. The interactions and scheduling between the  
2 microprocessor and the selector device may be embedded in either  
3 system or otherwise shared between the systems. Wherein multiple  
4 memory areas may be active and multiple memory areas are  
5 inactive, multiple memory areas may be updated and all  
6 corresponding entry points changed within the same selector  
7 device modification.

8 Many additional changes in the details, materials, steps and  
9 arrangement of parts, herein described and illustrated to explain  
10 the nature of the invention, may be made by those skilled in the  
11 art within the principle and scope of the invention.

12 Accordingly, it will be understood that the invention is not to  
13 be limited to the embodiments disclosed herein, may be practiced  
14 otherwise than specifically described, and is to be understood  
15 from the following claims, that are to be interpreted as broadly  
16 as allowed under the law.

I claim:

1. A method for modifying memory on at least one control device, from a remote host device, without interrupting the operation of the control device, wherein the control device and the host device are coupled through a Fieldbus communications network, the method comprising:

transferring data from the host device to the control device during unscheduled communications periods;

storing the transferred data to an inactive memory area;  
and,

redirecting at least one control instrument microprocessor, during a microprocessor idle period, to execute the stored data in the inactive memory area.

2. A method according to claim 1, further comprising verifying the stored data in the inactive memory areas.

3. A method according to claim 1, wherein redirecting the microprocessor further comprises providing the microprocessor with entry points to the stored data.



4. A method according to claim 1, wherein transferring data further comprises transmitting entry points.
5. A method according to claim 1, wherein transferring data further comprises transmitting executable instructions.
6. A method according to claim 1, wherein transferring data further comprises synchronizing data transmissions between the host device and the control devices to avoid interference with scheduled communications.
7. A method according to claim 1, further comprising:
  - selecting at least one active memory area; and,
  - inactivating the selected active memory area such that the microprocessor does not execute data in the selected active memory area.
8. A method according to claim 1, wherein redirecting the microprocessor further comprises issuing an upgrade request from the host device to the control devices.

9. A method according to claim 8, wherein issuing an upgrade request further comprises coordinating at least one upgrade command from the host device to at least one control device.

10 A method according to claim 1, wherein redirecting the microprocessor further comprises:

monitoring at least one parameter; and,

communicating a command to redirect the microprocessor when the parameter attains a specified value.

11. A system for modifying memory on at least one control device, from a remote host device, without interrupting the operation of the control device, wherein the control device and the host device are coupled through a Fieldbus communications network, the system comprising:

at least one control device, the control devices further comprising at least one active memory area and at least one inactive memory area;

at least one control device microprocessor to execute instructions and data in the active memory areas; and,

a control device selector module to direct the microprocessor to at least one active memory area, the selector module further comprising a scheduling module to redirect the microprocessor during microprocessor idle periods.

12. A system according to claim 11, wherein the selector module further comprises entry points to direct the microprocessor.

13. A system according to claim 11, wherein the microprocessor further comprises a memory verification module.

14. A system according to claim 11, wherein:

the active memory area comprises flash memory; and,

the inactive memory area comprises flash memory.

15. A system according to claim 11, wherein the host device further comprises:

a Fieldbus communications module to access the Fieldbus communications network;

a control module to receive, transmit, and display commands and data between the Fieldbus communications network and a host device user; and,

a control device communications module to transmit and receive commands and data between the host device and the control device.

16. A system according to claim 15, wherein the control module further comprises a user interface.

17. A system according to claim 11, wherein the host device is a microprocessor-based device.

18. A system according to claim 11, wherein:

the active memory data comprises executable instructions and data; and,

the inactive memory data comprises executable instructions and data.

1/4

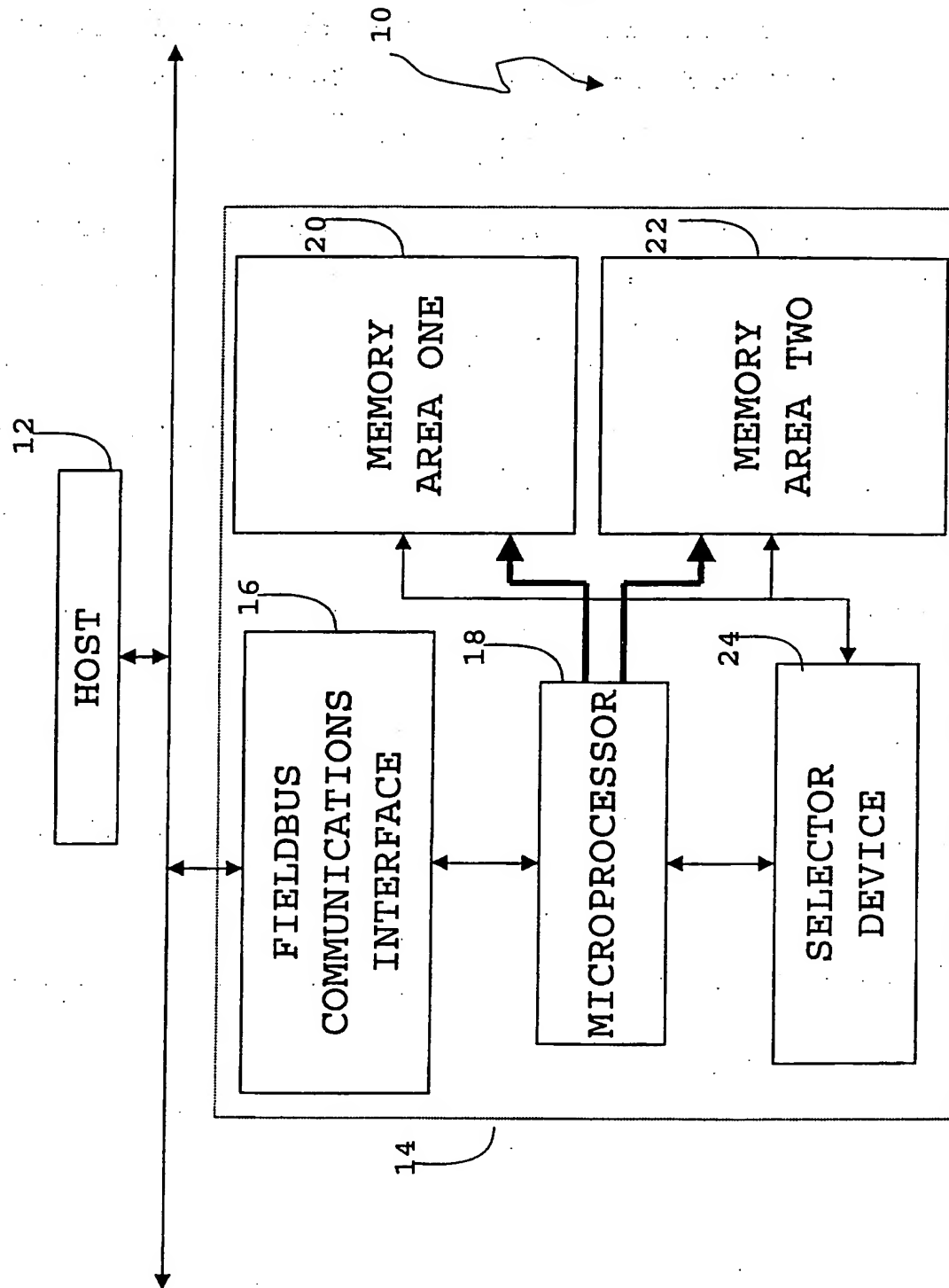


FIG. 1

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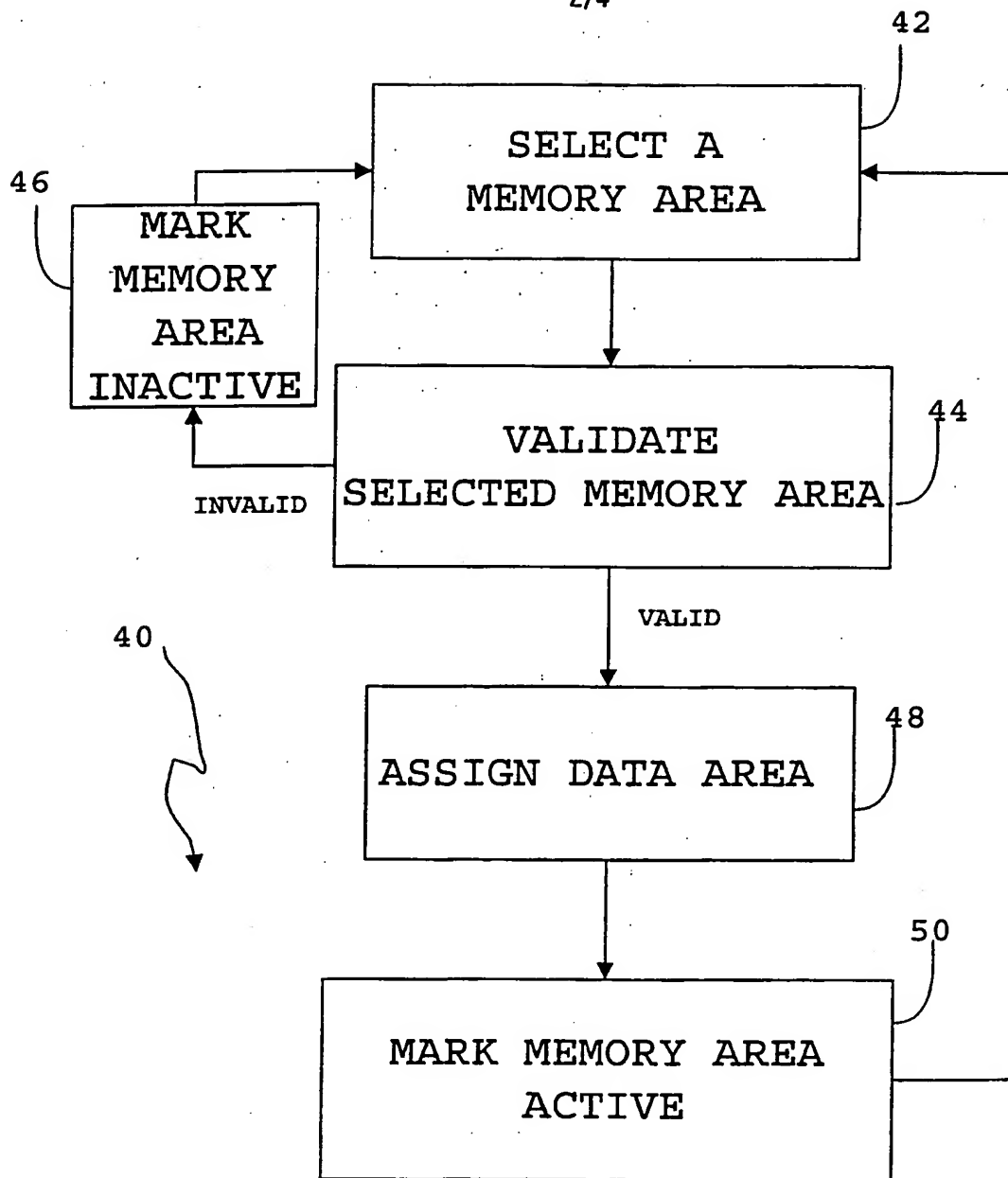


FIG. 2

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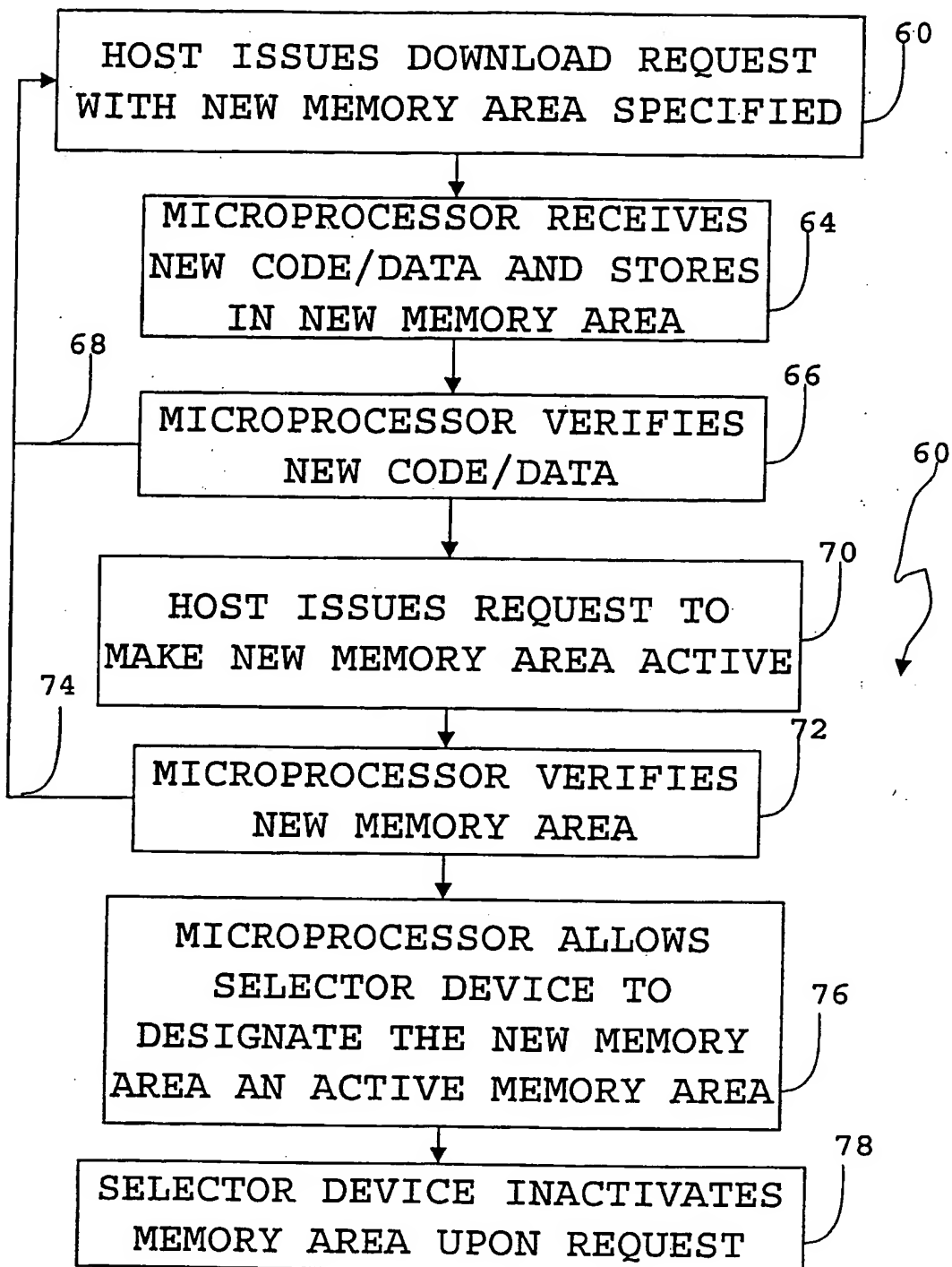


FIG. 3

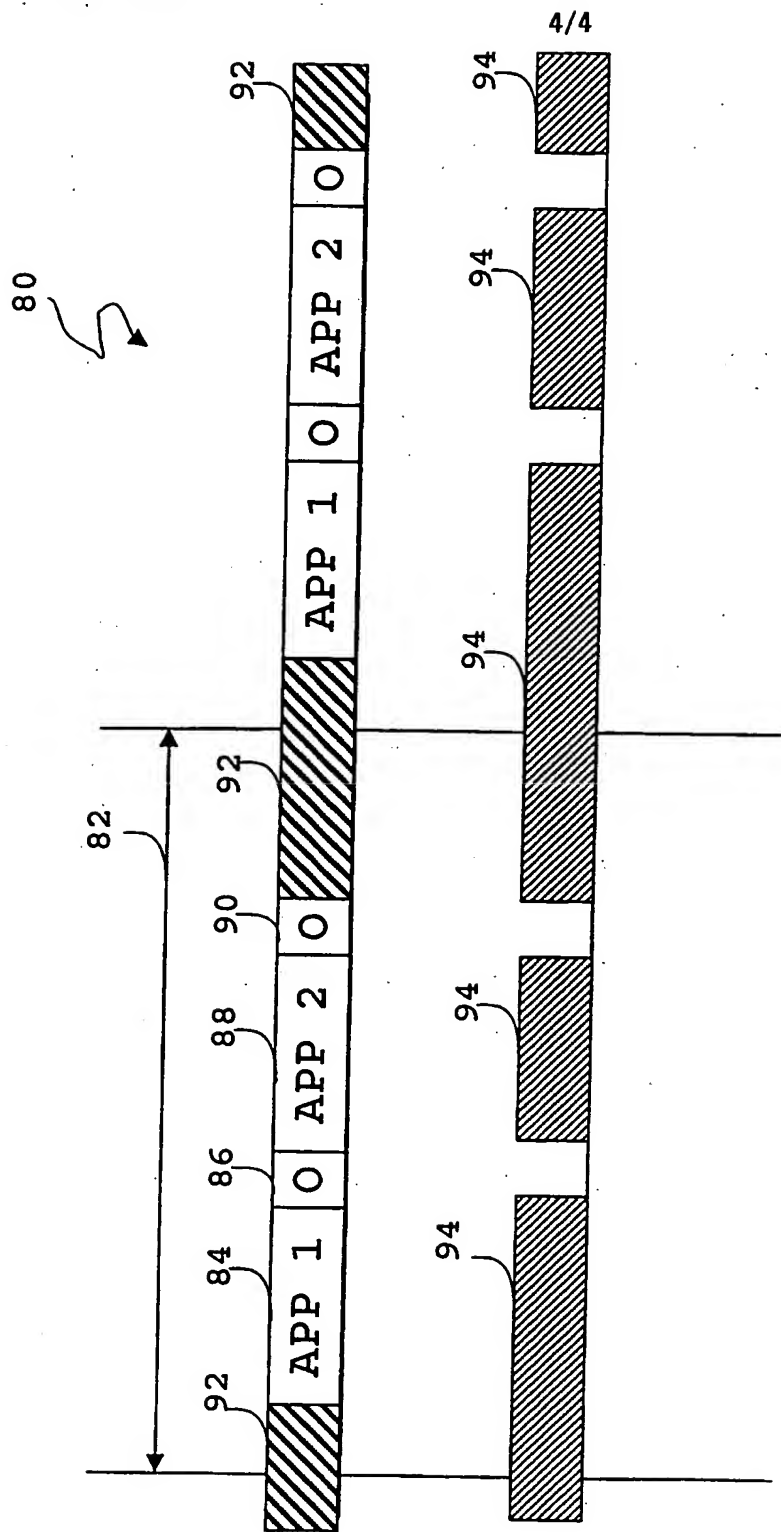


FIG. 4



# INTERNATIONAL SEARCH REPORT

International Application No.

PCT/US 00/14879

**A. CLASSIFICATION OF SUBJECT MATTER**  
IPC 7 G06F9/445

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, IBM-TDB

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 732 275 A (TITUS DIANE ET AL) 24 March 1998 (1998-03-24)	1,3,5,6, 11,12, 17,18
Y	column 3, line 58 -column 4, line 19	2,8-10, 13-16
A	column 5, line 49 - line 55 column 6, line 42 - line 49	4,7
A	WO 98 53619 A (ERICSSON TELEFON AB L M) 26 November 1998 (1998-11-26)	1,3,5-8, 10-12, 17,18
	column 5, line 17 -column 8, line 5	
Y	US 5 155 837 A (LO DANIEL S ET AL) 13 October 1992 (1992-10-13)	2,13
	column 7, line 63 -column 8, line 14	
	-/-	

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

\* Special categories of cited documents :

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"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"B" document member of the same patent family

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# INTERNATIONAL SEARCH REPORT

Internat Application No  
PCT/US 00/14879

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 96 18146 A (ERICSSON TELEFON AB L M ;FUCHS ROBERT (SE); HOLTE ROST ANNA (SE);) 13 June 1996 (1996-06-13) page 14, line 27 -page 18, line 26 -----	8,9
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Information on patent family members

International Application No

PCT/US 00/14879

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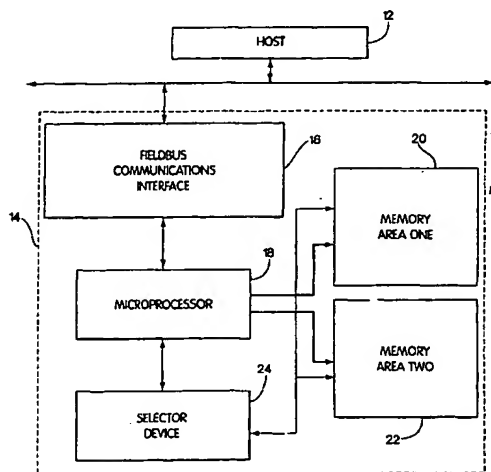
20 June 2002

(15) Information about Correction:

see PCT Gazette No. 25/2002 of 20 June 2002, Section II

[Continued on next page]

(54) Title: FIELDBUS UPGRADABLE APPARATUS AND METHOD



(57) Abstract: A method to modify control devices residing on a Fieldbus communications network, without interrupting the operation of the control devices. The control device updating may further be controlled and monitored by a remotely located host. The control device comprises at least two distinct memory areas wherein at least one memory area must be active, and at least one memory area must be inactive. Active memory areas provide the control device microprocessor operating system with executable instructions or data. The host downloads new executable instructions or data to inactivate memory areas, with associated data entry points, during unscheduled communications periods. Upon a full data transfer and proper verification of the new data, the host causes a selector device to activate the previously inactive memory area by directing the microprocessor to the entry points of the newly downloaded executable instructions or data. The memory activation must occur while the microprocessor is idle.



*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

1  
2                   FIELDBUS UPGRADABLE APPARATUS AND METHOD

3  
4                   CLAIM OF PRIORITY

5           This application claims priority to provisional  
6 application U.S.S.N. 60/136,253, entitled FIELDBUS UPGRADABLE  
7 DEVICE, and filed on May 27, 1999, naming VLADIMIR KOSTADINOV  
8 as inventor, the contents of which are herein incorporated by  
9 reference.  
10

11                   BACKGROUND OF THE INVENTION

12   (1) Field of the Invention

13           The present invention relates generally to communications  
14 systems, and more particularly to utilizing communications  
15 systems for uninterruptive software upgrading.

16   (2) Description of the Prior Art

17           In the manufacturing and process control industries,  
18 there is a continuing effort to eliminate older, centralized  
19 plant control strategies, in favor of standard protocols.  
20 This type of control provides true device interoperability,  
21 enhanced field-level control, and reduced installation costs.

22           The inherent modularity and intrinsic software reliance  
23 of modern manufacturing and process control systems allows a  
24 platform wherein distributed control may be best utilized.  
25 Communications protocols such as the commonly known Fieldbus  
26 technology allow for the interconnecting of measurement and  
27 control equipment such as sensors, actuators, and controllers.

28   Examples of some Fieldbus technologies include Profibus™ and

1 Foundation™. Fieldbus is an all-digital, serial, two-way  
2 communications system that serves as a Local Area Network  
3 (LAN) for instruments in process control and manufacturing  
4 automation applications. Fieldbus facilitates the  
5 distribution of the control application across the network.  
6 Control through the network is particularly advantageous when  
7 the devices or processes to be controlled are physically  
8 remote from a central control station.

9 Although the systems, sensors, and devices of such  
10 manufacturing and process systems are modular, and there are  
11 communications standards for interconnecting components of  
12 such systems, there is currently no method or apparatus for  
13 allowing device, system, or sensor software upgrades from  
14 remote locations without interrupting the control system.

15 What is needed is a method and apparatus that facilitates  
16 uninterrupted and remote upgrade of specified control system  
17 components.

18

19 SUMMARY OF THE INVENTION

20 It is one aspect of the present invention to provide a  
21 method and system for utilization with the well-known Fieldbus  
22 communication protocol, that allows uninterrupted software  
23 upgrading of remote, microprocessor controlled devices that  
24 exist on the Fieldbus network.

25 In a preferred embodiment, the Fieldbus network comprises  
26 a plurality of control devices, wherein control devices may be  
27 input devices, output devices, or input/output devices. Each  
28 control device may be configured for Fieldbus communications.

1 Each control device also comprises at least two memory areas  
2 within which executable software and data may reside, wherein  
3 at least one memory area may be active and at least one memory  
4 area may be inactive. Memory areas may further comprise  
5 multiple memory segments. Each control device additionally  
6 comprises a selector device that specifies to the  
7 microprocessor those memory areas that are active. In a  
8 preferred embodiment, the selector device directs the control  
9 device microprocessor to the active memory areas during the  
10 microprocessor operating system cycle.

11 It is another aspect of the present invention to allow a  
12 Fieldbus communications system wherein a host computer  
13 configured within the Fieldbus network may provide software  
14 upgrades and other control to remote control devices through  
15 the network. In an embodiment, software upgrades are  
16 performed without interrupting the control device processor,  
17 by issuing a Fieldbus compatible command that indicates to the  
18 control device microprocessor that a new software version is  
19 available for the designated control device. The respective  
20 microprocessor routes the software upgrade to a presently  
21 inactive memory area within the designated control device that  
22 shall be designated the new memory area. Such transfer occurs  
23 during otherwise unscheduled communications periods to avoid  
24 interruption to the network or the control device. Similarly,  
25 the remotely located control device microprocessor performs  
26 the transfer without interrupting the presently executing  
27 application or data functions in the control device. The  
28 microprocessor also verifies the new software. The new memory



1 area may be activated during a microprocessor idle period by  
2 directing the microprocessor to the new software, thereby  
3 providing a seamless transition to the new memory area and  
4 hence the new software.

5 It is another aspect of the invention to provide a  
6 mechanism whereby the host may return the microprocessor to a  
7 previously active memory area within a designated control  
8 device.

9 It is yet another aspect of the invention to utilize new  
10 memory areas for increasing the control device functionality.

11 The number of active memory areas may increase as  
12 functionality is increased.

13 Other objects and advantages of the present invention  
14 will become more obvious hereinafter in the specification and  
15 drawings.

16

17

1                    BRIEF DESCRIPTION OF THE DRAWINGS

2        A more complete understanding of the invention and many  
3        of the attendant advantages thereto will be readily  
4        appreciated as the same becomes better understood by reference  
5        to the following detailed description when considered in  
6        conjunction with the accompanying drawings, wherein like  
7        reference numerals refer to like parts and wherein:

8            FIG. 1 is a representative block diagram of a Fieldbus  
9        communications network segment displaying a host and a single  
10       control device;

11          FIG. 2 presents a control device initialization  
12       methodology;

13          FIG. 3 diagrammatically represents the logic for altering  
14       control device memory; and,

15          FIG. 4 presents the microprocessor operating system and  
16       unscheduled communications timelines.

17

18                    DESCRIPTION OF THE PREFERRED EMBODIMENT

19        To provide an overall understanding of the invention,  
20        certain illustrative embodiments will now be described;  
21        however, it will be understood by one of ordinary skill in the  
22        art that the systems described herein can be adapted and  
23        modified to provide systems for other suitable applications  
24        and that other additions and modifications can be made to the  
25        invention without departing from the scope hereof.

26        Referring now to FIG. 1, there is shown a block diagram  
27        of a system 10 that incorporates an embodiment of the  
28        invention. The FIG. 1 system 10 comprises a host 12 that is

1 configured for communications using the well-known Fieldbus  
2 communications protocol. The host 12 can be implemented using  
3 a digital computer system that may be any microprocessor-based  
4 system including a computer workstation, such as a PC  
5 workstation, SUN workstation, handheld or laptop computer,  
6 that comprises a program for organizing and controlling the  
7 digital computer system to operate according to the invention.  
8 Additionally and optionally, the microprocessor-based system  
9 can be equipped for processing multimedia data, and can be,  
10 for example, a conventional PC computer system with a sound  
11 and video card. The computer system can operate as a stand-  
12 alone system when not operating as part of a networked  
13 computer system. The host may therefore be any  
14 microprocessor-based device that is designated to perform the  
15 functionality herein to uninterruptively upgrade software on a  
16 specified control device, such specified control device  
17 including, for example, a field device such as a controller,  
18 transmitter, or actuator.

19 The host 12 may provide and receive remote command and  
20 control information to and from a plurality of control devices  
21 residing on the network. FIG. 1 displays a representative  
22 control device 14. The host 12 and control device 14 may not  
23 be co-located on the same Fieldbus segment, and communications  
24 between the host 12 and control device 14 may be coupled  
25 through various Fieldbus and other network segments, that  
26 shall be referred to herein collectively as the Fieldbus  
27 communications network.

1 Control devices may be input devices, output devices, or  
2 input/output devices as commonly known in the art. As  
3 indicated by FIG. 1, the control device comprises a Fieldbus  
4 communications interface 16 to receive and transmit commands  
5 and data across the Fieldbus network, at least one  
6 microprocessor 18 to execute control device resident  
7 applications and communicate with the host and other control  
8 devices, at least two memory areas 20, 22 for storing  
9 executable programs and/or data that may be accessed by the  
10 microprocessor 18, and a selector device 24 interfaces the  
11 microprocessor 18 to executable instructions or data in the  
12 memory areas 20, 22.

13 In a preferred embodiment, the memory areas 20, 22 may be  
14 flash memory, although other memory devices may be utilized  
15 without departing from the invention. Each memory area 20, 22  
16 may additionally be continuous, partitioned, or segmented.  
17 The FIG. 1 memory areas 20, 22 therefore merely represent  
18 logically separate memory areas, and each memory area 20, 22  
19 may be comprised of memory across multiple segments, etc.

20 For the purposes of this invention, all references to the  
21 microprocessor 18 shall be understood to refer to the embedded  
22 software or operating system that forms a microprocessor  
23 operating system, wherein such an operating system is commonly  
24 known for scheduling and executing applications, allocating  
25 resources, etc. In a preferred embodiment, the microprocessor  
26 18 repeatedly performs a scheduled series of tasks during a  
27 fixed time period. The tasks are identified to the  
28 microprocessor 18 through entry points that specify a memory

1 area, wherein the memory area comprises executable  
2 instructions or data to perform and/or complete the task. In  
3 an embodiment, the memory area may comprise executable  
4 instructions or data relating to a control device application.

5 For purposes of this invention, each such repetitive  
6 fixed time period wherein the microprocessor performs the  
7 scheduled tasks shall be defined as a macrocycle.  
8 Additionally, any time within the macrocycle during which the  
9 microprocessor is not executing an application, performing  
10 application-dependent input/output, or performing application  
11 related communications, shall be defined as an idle period.

12 As FIG. 1 indicates, the microprocessor 18 may access the  
13 memory areas 20, 22 in two manners for two distinct purposes.

14 The microprocessor connection to the memory areas 20, 22  
15 through the selector device 24 represents the selector device  
16 functionality to supply the microprocessor 18 with entry  
17 points for application executable instructions or data,  
18 wherein such application instructions or data resides in the  
19 memory areas 20, 22. For the purpose of this invention, such  
20 activity shall be defined as "executable" activity, wherein  
21 the microprocessor 18 executes the instructions or data  
22 residing in the memory areas 20, 22.

23 Alternately, the microprocessor 18 may directly access  
24 the memory areas 20, 22 (i.e., without selector device 24  
25 intervention) to perform functions unrelated to application or  
26 data execution. Examples of such functions include data  
27 integrity checks, data loading or unloading, etc. For  
28 purposes of this invention, such activity shall be defined as

1 "processing" activity, wherein the microprocessor 18 processes  
2 the memory area contents without executing the instructions or  
3 data therein.

4 The selector device 24 may designate an active memory  
5 area(s) from an inactive memory area(s) for the microprocessor  
6 18. For the purposes of this invention, active memory areas  
7 shall be defined as the memory areas that the microprocessor  
8 18 is directed to, by the selector device 24, to obtain  
9 executable instructions or data. In a preferred embodiment,  
10 the selector device 24 activates a memory area merely by  
11 providing the microprocessor 18 with the entry points to the  
12 memory area.

13 For purposes of this invention, all memory areas other  
14 than the active memory areas shall be known as inactive memory  
15 areas. The microprocessor 18 does not execute instructions or  
16 data from any inactive memory area, however the microprocessor  
17 may process the inactive memory area contents for data  
18 integrity, perform data downloading, etc.

19 For purposes of this invention, a new memory area shall  
20 be defined as an inactive memory area to which upgradeable  
21 executable instructions (e.g., an application) or data shall  
22 be directed, wherein such upgradeable instructions or data  
23 shall also be referred to collectively as new data. New data  
24 may work independently, to the exclusion of, or together with,  
25 existing data in active memory areas.

26 In a preferred embodiment, the selector device 24 is  
27 incorporated as a software module that interacts with the  
28 microprocessor 18 and may be implemented through software

1 using higher-level languages such as C++ or Java, or  
2 optionally microcode or machine level instructions; however,  
3 those with ordinary skill in the art shall recognize that the  
4 selector device 24 may be implemented in hardware without  
5 departing from the scope of the invention herein.

6 Referring now to FIG. 2, there is shown a representative  
7 process 40 by which a control device may be initialized. In  
8 an embodiment presented in FIG. 2, upon initialization, the  
9 control device cycles through all control device memory areas  
10 and sets to active all memory areas that are verified through  
11 the verification process. In such an embodiment, the control  
12 device microprocessor selects, in a logical order, a memory  
13 area 42. The microprocessor may then verify 44 the memory  
14 area contents using such well-known techniques as CRC  
15 computations, although the invention is not limited by such  
16 verification technique. If the verification fails, the memory  
17 area may be marked as inactive 46, and another memory area is  
18 selected 42. In a preferred embodiment, such inactive  
19 designation 46 may be a passive activity since all memory  
20 areas other than the active memory area may be by default,  
21 inactive; however, alternate embodiments may otherwise  
22 designate inactive memory areas using alternate techniques  
23 without departing from the invention herein.

24 Alternately, when a memory area is properly verified, a  
25 data area may be assigned 48 within the memory area, and the  
26 memory area may be designated active 50. The next memory area  
27 in the logical order may then be selected 42, until all such  
28 memory areas are designated active or inactive.

1        Although FIG. 2 presents an initialization process for  
2        one embodiment wherein multiple memory areas may be active,  
3        alternate embodiments may utilize different initialization  
4        processes. In applications wherein only one memory area may  
5        be allowed to be active, such memory area may be "selected" 42  
6        by the respective selector device or microprocessor that may  
7        retain or preserve the active and inactive memory area status  
8        data from a previous session. In yet another embodiment, the  
9        host may store the location of the active memory areas for  
10       each control device, and transmit, using the Fieldbus  
11       protocol, the active memory address(es) to the respective  
12       control device upon initialization.

13       Referring now to FIG. 3, there is shown a process 60  
14       wherein new executable instructions or data may be provided to  
15       a designated control device. In the FIG. 3 embodiment,  
16       updating the control device comprises downloading new data.  
17       The host may request an upgrade to the control device, and the  
18       request may be communicated between the host and control  
19       device using Fieldbus protocols. As FIG. 1 indicates,  
20       communications between the host and the control device require  
21       communication through the Fieldbus interface, that thereafter  
22       interacts with the microprocessor that processes the commands.

23       Such communications may occur during otherwise unscheduled  
24       communications periods between the host and control device,  
25       wherein unscheduled communications periods may be defined as  
26       those time periods during which the control device  
27       microprocessor may not be previously scheduled to exchange  
28       input/output data relating to applications executing on the



1 control device. Such previously scheduled input/output  
2 periods may comprise communications between the control device  
3 and the host, or between the control device and another  
4 control device.

5       The host may identify the control device through a user-  
6 interface or other interactive mechanism that allows a host  
7 operator to designate a specific control device. In a  
8 preferred embodiment, the host comprises a user interface that  
9 similarly indicates respective active and inactive memory  
10 areas for specified control devices. The host may store  
11 information regarding the present active memory areas for a  
12 specified control device and display such information to the  
13 host user, or alternately, the host may poll the selector  
14 device of the specified control device, using the Fieldbus  
15 protocol, to ascertain the present active memory areas. In  
16 yet another embodiment, the selector device may provide the  
17 host with the active memory area designation upon completion  
18 of the control device initialization processing as indicated  
19 by FIG. 2.

20       In a preferred embodiment, the host user interface may  
21 allow a host operator to specify an inactive memory area as a  
22 target for the new data. Such user interface may also allow  
23 the host operator to specify the new data. Referring back to  
24 FIG. 3, the host may then issue, using Fieldbus communications  
25 protocols, a data download request 62 that may be received by  
26 the specified control device microprocessor to cause the new  
27 memory area identifier and new data to be transmitted to the  
28 control device. In a preferred embodiment, the host also

1 transfers the new memory area entry points, wherein the entry  
2 points shall direct the microprocessor to the executable  
3 instructions or data in the new memory area. Such host  
4 requests and transfers are also performed during previously  
5 defined unscheduled communications intervals.

6     Upon receipt 64 of the download request and new memory  
7 area designation, new data, and new memory area entry points,  
8 the microprocessor may direct the new data to the new memory  
9 for storage. The microprocessor may also direct the new  
10 memory entry points to the selector device for storage. The  
11 host may then issue a verification command that may cause the  
12 control device microprocessor to verify 66 the new data in the  
13 new memory area, wherein such verification may be, for  
14 example, a CRC computation, but the invention herein is not  
15 limited to such verification method. In an embodiment, the  
16 microprocessor stores the result of such memory verification  
17 in the selector device. In a preferred embodiment, the  
18 microprocessor functions of receiving 64, redirecting 64, and  
19 verifying 66 the new data, may be performed in parallel  
20 processes with the presently executing applications in the  
21 active memory areas. Such functions may therefore be  
22 performed at any time in the microprocessor timeline, other  
23 than the during scheduled input/output network communications  
24 intervals.

25     If a proper verification of the new memory area is not  
26 achieved 68, the host may issue another download request,  
27 again designating a new memory area and the new data. The  
28 same inactive memory area may be utilized, or the host may

1 request a different memory area if more than one inactive  
2 memory areas exist.

3 Alternately, upon proper verification of a memory area,  
4 the control device microprocessor may inform the host of the  
5 proper verification, wherein the host may request that the new  
6 memory be designated an active memory 70.

7 The control device microprocessor, upon receiving a  
8 request from the host to change the status of an inactive  
9 (i.e., new) memory area to active, may interrogate the  
10 verification status of the new memory 72. Alternately, the  
11 microprocessor may interrogate whether entry points are  
12 received for the new memory area. If the new memory area is  
13 not verified, or entry points do not exist, the microprocessor  
14 may reject 74 the host request to change the active memory  
15 designation. Alternately, if the new memory is verified and  
16 entry points are stored, the host's request may be granted,  
17 and the microprocessor may inform the selector device that the  
18 new memory area may be activated 76.

19 Depending upon, for example, whether the new data  
20 comprises cooperative as compared to replacement data, the  
21 host may issue a request to inactivate a presently active  
22 memory area 78. In some embodiments, activating and  
23 inactivating memory areas may require proper coordination and  
24 timing to achieve the desired microprocessor direction via the  
25 selector device-provided entry points.

26 In one embodiment wherein the system is initialized  
27 through the cyclic process depicted in FIG. 2, memory  
28 inactivation may cause the memory area to purposefully fail

1 subsequent verification checks. In such a system, re-  
2 activating the content of that memory segment may require a  
3 new download of the older executable instructions or data.  
4 Alternately, the inactivation process may be reversible with  
5 another command from the host, thereby preventing the  
6 necessity for another data download.

7 In embodiments wherein only one memory area can be  
8 active, the inactivation process may be simplified and may be  
9 implemented using default logic embedded in software or  
10 hardware. All such activation and inactivation methods and  
11 processes may be implemented in various manners without  
12 departing from the scope of the present invention.

13 The method of indicating active or inactive memory areas  
14 relates also to the ability to return to previous versions of  
15 executable instructions or data. For example, if a system  
16 comprises N memory areas, wherein only one memory area may be  
17 active, the system may be implemented such that as many as (N-  
18 1) versions of executable instructions or data may be stored  
19 in inactive memory areas. Such configuration may also allow  
20 rapid transition between these versions of executable  
21 instructions or data by issuing a host request with the new  
22 memory area designation.

23 Alternately, when multiple memory areas are allowed to be  
24 active, the present invention provides a structure wherein  
25 functionality may be easily added or eliminated. Modular  
26 upgrades may also be readily achieved in such an embodiment,  
27 wherein one memory area with a specific functionality may be  
28 upgraded to the exclusion of other active memory areas.

1        Referring now to FIG. 4, there is shown two timelines 80  
2        indicating a representative microprocessor operating system  
3        timeline, previously defined as a macrocycle, and a  
4        corresponding unscheduled communications timeline. As  
5        mentioned previously, the macrocycle 82 may be viewed as a  
6        repeatable interval, the duration of which may be designed to  
7        allow execution of all control device applications and  
8        input/output functions, with consideration for the overall  
9        communications bandwidth during the input/output functions.  
10       For example, during each representative macrocycle of FIG. 4,  
11       the microprocessor operating system executes a first  
12       application 84, wherein such first application is followed  
13       immediately by a first input/output interval 86. During the  
14       first input/output interval 86, the control device may  
15       transfer data relating to the first application, using the  
16       Fieldbus protocol. Such communications intervals 86 are  
17       therefore known as scheduled communications intervals, and may  
18       be between the control device and the host, or between the  
19       control device and another control device. Upon completion of  
20       the first input/output interval 86, the microprocessor  
21       executes a second application 88, wherein such second  
22       application 88 is followed in time by a second input/output  
23       interval 90, such second input/output interval 90 also being a  
24       scheduled communications interval. Although the  
25       representative embodiment of FIG. 4 indicates only two  
26       applications, the invention herein is not limited by the  
27       number of applications executed on a control device during a  
28       given macrocycle.

1 Referring again to FIG. 4, the selector device may  
2 activate or inactivate memory areas, or change the entry  
3 points, at any time during the macrocycle that the  
4 microprocessor operating system is not executing applications  
5 or utilizing application dependent data. Such periods in the  
6 macrocycle are indicative of the previously defined idle  
7 periods 92. During these idle periods 92, the selector device  
8 may incorporate the entry points to the new memory area such  
9 that during the microprocessor's next scheduled application  
10 execution, the new entry points may direct the microprocessor  
11 to the new data. By altering the microprocessor entry points  
12 during intervals wherein the microprocessor is not performing  
13 application or application-dependent processing, the  
14 transition to the new data may occur without interrupting the  
15 microprocessor functionality or processing timeline.

16 As mentioned previously, activating a memory area may  
17 require inactivating another memory area, and such  
18 activation/inactivation may require coordination.  
19 Inactivation, just as activation, must be performed during the  
20 idle periods 92, when the microprocessor is neither scheduled  
21 for application execution or application input/output. Such  
22 activation/inactivation may require several idle periods to  
23 achieve complete conformance. In an embodiment, the host may  
24 extend an idle period (i.e., prevent the next macrocycle from  
25 commencing) to effectuate a memory area activation or  
26 inactivation.

27 Alternately, data transfers from the host computer to the  
28 new memory area, or any commands or requests from the host,

1 may be scheduled during the unscheduled communications periods  
2 94. As defined previously, unscheduled communications periods  
3 94 comprise any macrocycle time interval during which the  
4 microprocessor is not performing input/output with the host or  
5 another control device. Unscheduled communications therefore  
6 comprise all time within the processing interval that is not a  
7 scheduled communications interval.

8 As with any communications system, data rates must be  
9 considered when scheduling events. Depending upon the data  
10 rates and the data amount transferred to a new memory area,  
11 more than one macrocycle may be required to download the data;  
12 therefore, the download of executable instructions or data to  
13 a new memory area may occur during one macrocycle, while the  
14 verification of such new memory may not occur until several  
15 macrocycles after such download begins. Further, altering the  
16 microprocessor operating system entry points may require a  
17 period greater than a single idle period 92, thereby delaying  
18 the activation of a new memory area for several macrocycles.

19 In one embodiment where several control devices may be  
20 upgraded, the upgrades may be coordinated to occur at the same  
21 time. In such an embodiment, new data may be downloaded to  
22 all control devices, and respective microprocessors may be  
23 redirected to respective new data memory areas to achieve a  
24 synchronized or otherwise controlled upgrade.

25 In one embodiment, the microprocessor redirection for one  
26 or more control devices may be scheduled to a certain time or  
27 event, without departing from the invention. In such an  
28 embodiment, one or more control devices may comprise new data

1 in an inactive memory area. The host may then monitor at  
2 least one parameter, wherein the parameter(s) may relate to  
3 control devices, and upon the particular parameter(s)  
4 attaining a predetermined value, the host may issue a request  
5 to redirect the microprocessor on one or more control devices.

6 The advantage of the present invention over the prior art  
7 is that control devices within a Fieldbus network may be  
8 remotely updated with new executable instructions or data  
9 without disturbing the operation of the control device.

10 What has thus been described is a method and apparatus to  
11 modify control devices residing on a Fieldbus communications  
12 network, without interrupting the operation of the control  
13 devices. The control device updating may further be  
14 controlled and monitored by a remotely located host that also  
15 communicates on the Fieldbus network. The control device may  
16 comprise at least two distinct memory areas, wherein at least  
17 one memory area must be active, and at least one memory area  
18 must be inactive. Active memory areas provide the control  
19 device microprocessor operating system with executable  
20 instructions or data. The host downloads new executable  
21 instructions or data to inactive memory areas, with associated  
22 data entry points, during unscheduled communications periods  
23 wherein data input/output is not being performed between the  
24 control device and the host or another control device. Upon  
25 a full data transfer and proper verification of the new data,  
26 the host may issue an activation command that causes a  
27 selector device to activate the previously inactive memory  
28 area by directing the microprocessor to the entry points of



1 the newly downloaded executable instructions or data. The  
2 memory activation must occur while the microprocessor is not  
3 performing application execution, application input/output, or  
4 application communications. By timing the memory activation  
5 in this manner, the microprocessor may be redirected to the  
6 newly downloaded executable instructions or data without  
7 microprocessor interruption.

8       Although the present invention has been described  
9 relative to a specific embodiment thereof, it is not so  
10 limited. Obviously many modifications and variations of the  
11 present invention may become apparent in light of the above  
12 teachings. For example, the selector device functionality may  
13 be performed in hardware or software. The selector device may  
14 be incorporated within the microprocessor or independent of  
15 the microprocessor operating system. The Fieldbus network may  
16 contain any number of control devices. Each control device  
17 may have a different macrocycle length during which a varying  
18 number of applications may be executed. Depending on the  
19 network size, there may be more than one host. The host and  
20 the control devices may reside on different Fieldbus segments,  
21 wherein such segments may be connected through otherwise  
22 compatible network software or hardware. The interactions and  
23 scheduling between the microprocessor and the selector device  
24 may be embedded in either system or otherwise shared between  
25 the systems. Wherein multiple memory areas may be active and  
26 multiple memory areas are inactive, multiple memory areas may  
27 be updated and all corresponding entry points changed within  
28 the same selector device modification.

1       Many additional changes in the details, materials, steps  
2   and arrangement of parts, herein described and illustrated to  
3   explain the nature of the invention, may be made by those  
4   skilled in the art within the principle and scope of the  
5   invention. Accordingly, it will be understood that the  
6   invention is not to be limited to the embodiments disclosed  
7   herein, may be practiced otherwise than specifically  
8   described, and is to be understood from the following claims,  
9   that are to be interpreted as broadly as allowed under the  
10   law.

I claim:

1. A method for modifying memory on at least one control device, from a remote host device, without interrupting the operation of the control device, wherein the control device and the host device are coupled through a Fieldbus communications network, the method comprising:  
  
transferring data from the host device to the control device during unscheduled communications periods;  
  
storing the transferred data to an inactive memory area;  
  
and,  
  
redirecting at least one control instrument microprocessor, during a microprocessor idle period, to execute the stored data in the inactive memory area.
2. A method according to claim 1, further comprising verifying the stored data in the inactive memory areas.
3. A method according to claim 1, wherein redirecting the microprocessor further comprises providing the microprocessor with entry points to the stored data.
4. A method according to claim 1, wherein transferring data further comprises transmitting entry points.

5. A method according to claim 1, wherein transferring data further comprises transmitting executable instructions.

6. A method according to claim 1, wherein transferring data further comprises synchronizing data transmissions between the host device and the control devices to avoid interference with scheduled communications.

7. A method according to claim 1, further comprising:

selecting at least one active memory area; and,

inactivating the selected active memory area such that the microprocessor does not execute data in the selected active memory area.

8. A method according to claim 1, wherein redirecting the microprocessor further comprises issuing an upgrade request from the host device to the control devices.

9. A method according to claim 8, wherein issuing an upgrade request further comprises coordinating at least one upgrade command from the host device to at least one control device.

10. A method according to claim 1, wherein redirecting the microprocessor further comprises:

monitoring at least one parameter; and,

communicating a command to redirect the microprocessor  
when the parameter attains a specified value.

11. A system for modifying memory on at least one control device, from a remote host device, without interrupting the operation of the control device, wherein the control device and the host device are coupled through a Fieldbus communications network, the system comprising:

at least one control device, the control devices further comprising at least one active memory area and at least one inactive memory area;

at least one control device microprocessor to execute instructions and data in the active memory areas;  
and,

a control device selector module to direct the microprocessor to at least one active memory area, the selector module further comprising a scheduling module to redirect the microprocessor during microprocessor idle periods.

12. A system according to claim 11, wherein the selector module further comprises entry points to direct the microprocessor.

13. A system according to claim 11, wherein the microprocessor further comprises a memory verification module.

14. A system according to claim 11, wherein:

the active memory area comprises flash memory; and,

the inactive memory area comprises flash memory.

15. A system according to claim 11, wherein the host device further comprises:

a Fieldbus communications module to access the Fieldbus communications network;

a control module to receive, transmit, and display commands and data between the Fieldbus communications network and a host device user; and,

a control device communications module to transmit and receive commands and data between the host device and the control device.

16. A system according to claim 15, wherein the control module further comprises a user interface.

17. A system according to claim 11, wherein the host device is a microprocessor-based device.

18. A system according to claim 11, wherein:

the active memory data comprises executable instructions and data; and,

the inactive memory data comprises executable instructions and data.

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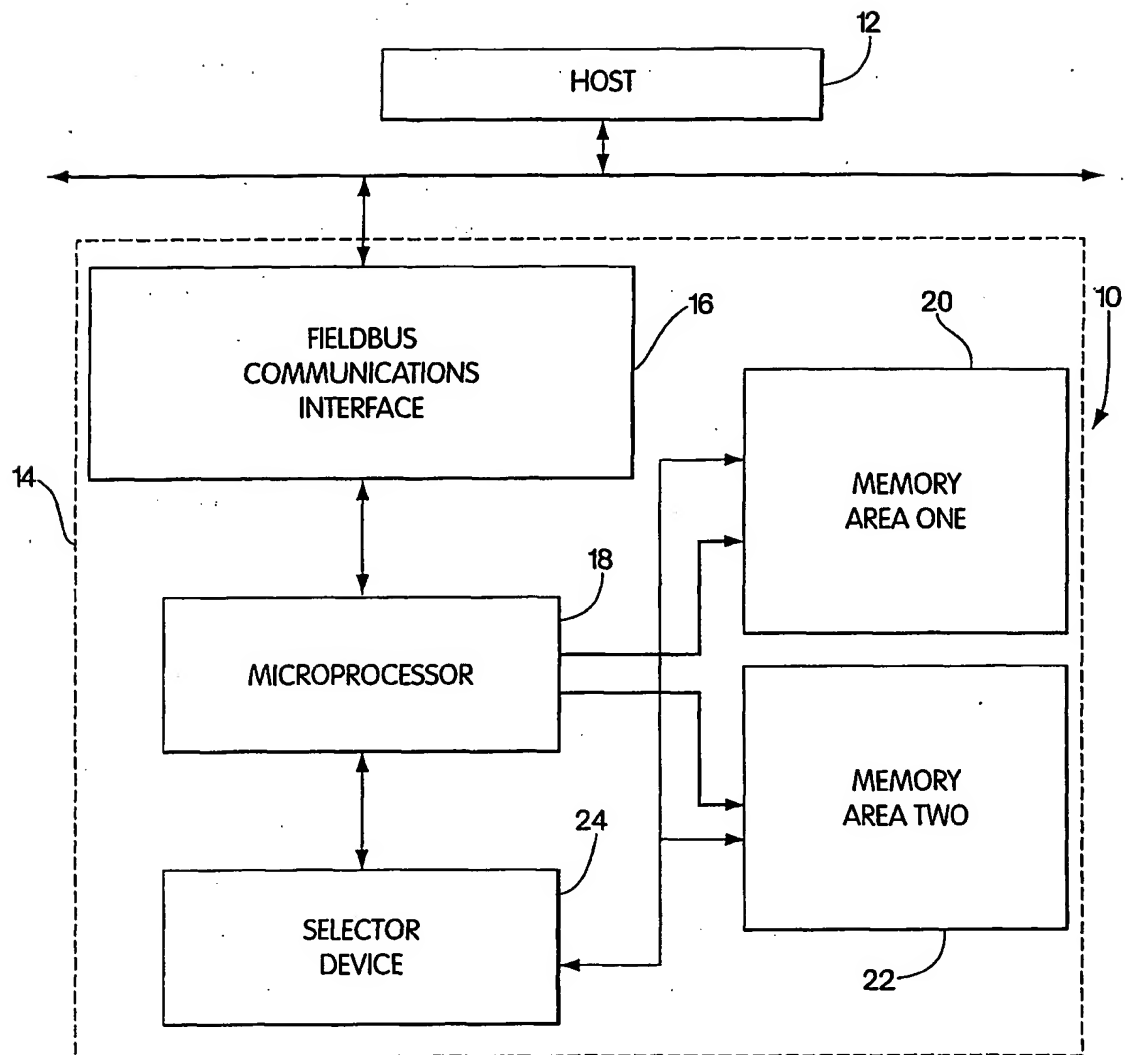


Fig. 1



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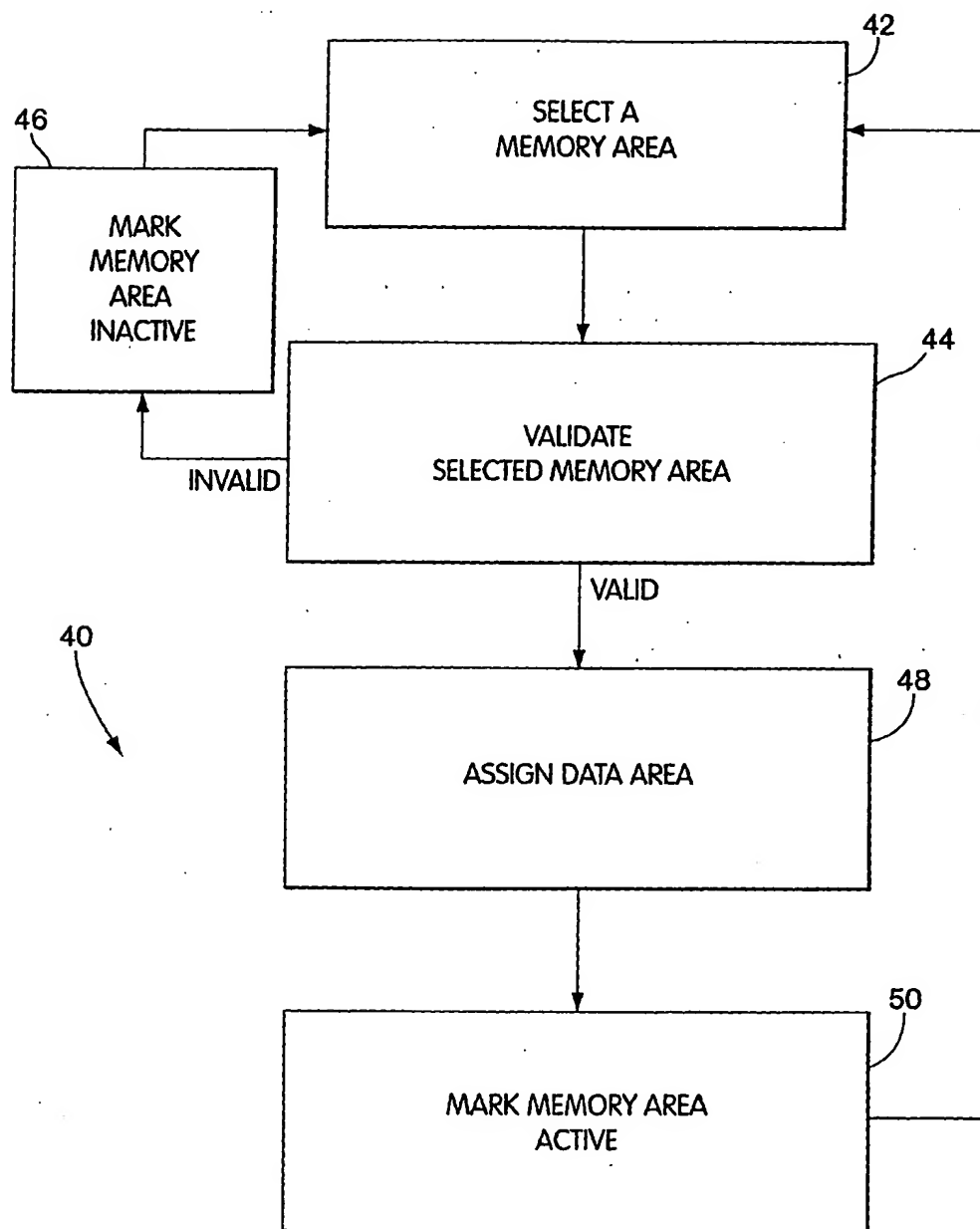


Fig. 2

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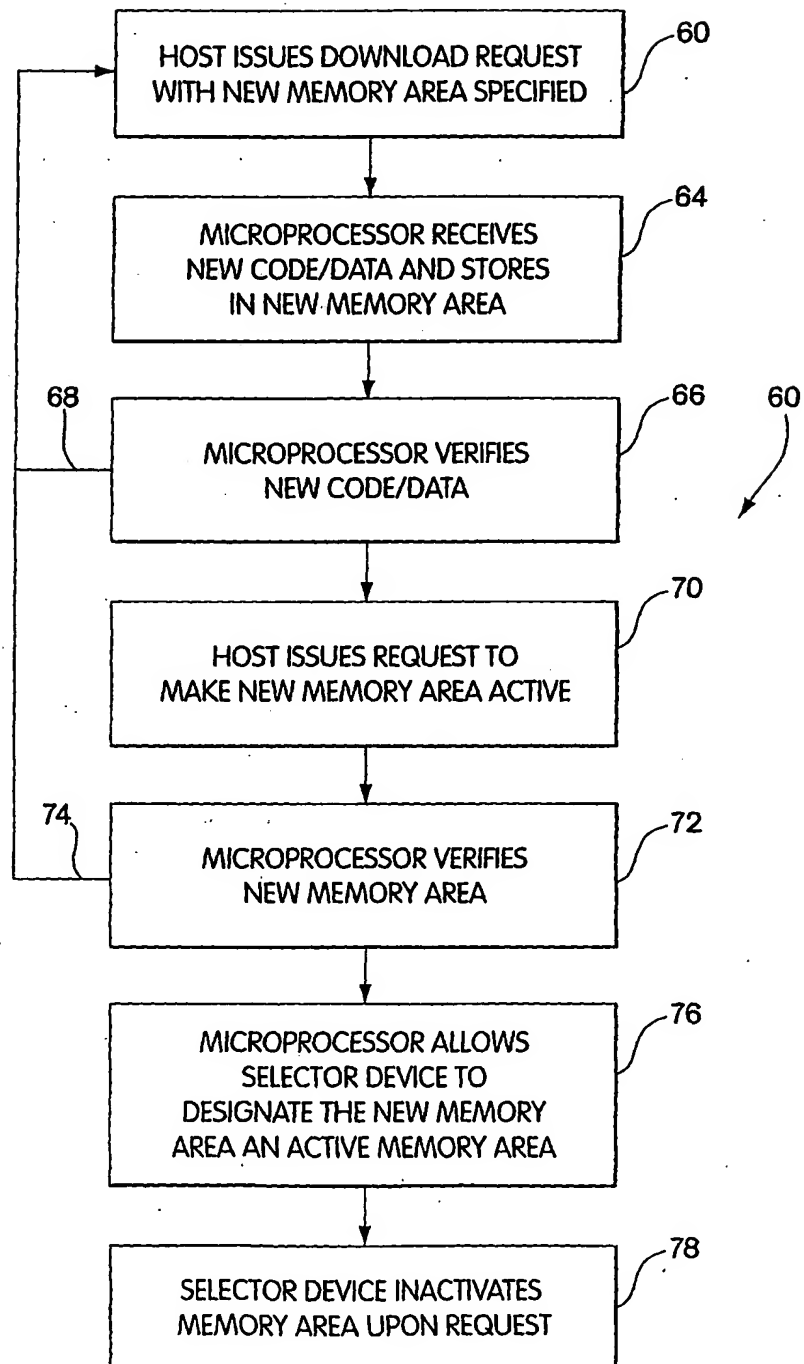


Fig. 3

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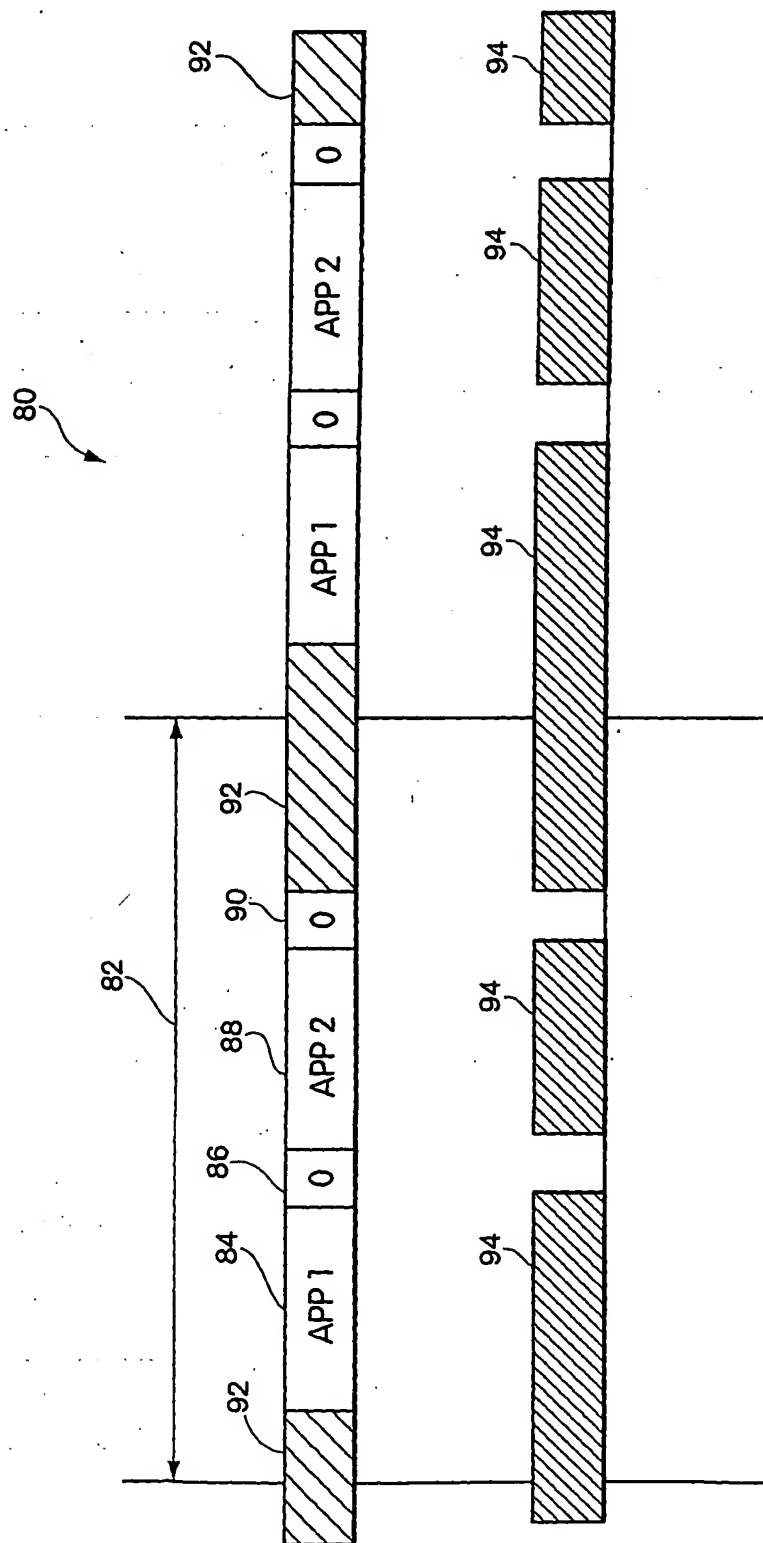


Fig. 4

# INTERNATIONAL SEARCH REPORT

International Application No.  
PCT/US 00/14879

## A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 G06F9/445

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, IBM-TDB

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	US 5 732 275 A (TITUS DIANE ET AL) 24 March 1998 (1998-03-24)	1,3,5,6, 11,12, 17,18
Y	column 3, line 58 -column 4, line 19	2,8-10, 13-16
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A	WO 98 53619 A (ERICSSON TELEFON AB L M) 26 November 1998 (1998-11-26)	1,3,5-8, 10-12, 17,18
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	column 7, line 63 -column 8, line 14	
	-/--	

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

### \* Special categories of cited documents :

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"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

10 November 2000

Date of mailing of the international search report

17/11/2000

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# INTERNATIONAL SEARCH REPORT

International Application No  
PCT/US 00/14879

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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